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Design of a Fully Integrated Three-Level Buck Converter

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Abstracts

Dynamic response of a converter plays an important role in many applications which change load in a rapid manner, especially in POL (Point of load) applicant ions. Here a new method for improving the dynamic response of a converter is presented. Here separate control schemes are implemented during steady state as well as transient load conditions. A three level buck converter topology with fast transient response is discussed here. This topology does not require a soft start up circuitry for three level buck converters. Simulation model is done in Matlab/Simulink and the result shows a great improvement in dynamic response of the system. The 3-level converter enables smaller inductors (1 NH) than a buck, while generating a wide range of output voltages compared to a 1/2 mode switched-capacitor converter. The test-chip prototype delivers up to 0.85 a load current while generating output voltages from 0.4 to 1.4 V from a 2.4 V input supply. It achieves 77% peak efficiency at power density of 0.1 W/mm and 63% efficiency at maximum power density of 0.3 W/mm.

Keywords: Buck DC-DC Converter, Three-level Buck converter.

Introduction

The dynamic response of a converter plays an important role in many areas like DSP based digital loads, point of load applications (PoL). Dynamic response is the performance of a converter during sudden load changes. The two important factors that should be considered during dynamic response are the peak overshoot as well as the recovery time. Many methods are proposed for improving the dynamic response of a system. In [3], a converter with two control strategies is proposed. PWM controller works at steady state condition and hysteresis controller which works at dynamic condition. Since hysteresis controller have its own disadvantages it is not suitable to use in all conditions. In [4] two buck converter topologies are cascaded each of them take care of two different conditions. The main disadvantage is that it requires more complex circuitry. A hysteresis controller is proposed in [6]. Some methods are proposed with change in the power stage of a converter to improve the dynamic response. In [7] a stepping inductance method is proposed. Here additional filter circuits are required and the system is complex as well. Three level buck converter topology is proposed here. This topology reduces the switching stress, inductor size and has high efficiency [2]. The buck converter circuit converts a higher dc input voltage to lower dc output voltage. A basic buck converter topology requires only one switch but it requires a large inductor value and switches work at very high frequency. So in the case of portable devices like mobiles the size should be less. In the case of multilevel converters, the switching frequency is reduced as well as the inductor size is also reduced, which in turn reduces the entire size of the converter as well. In section II three level buck converter topology is discussed. Section III suggests its control schemes. Simulations results are discussed in section.

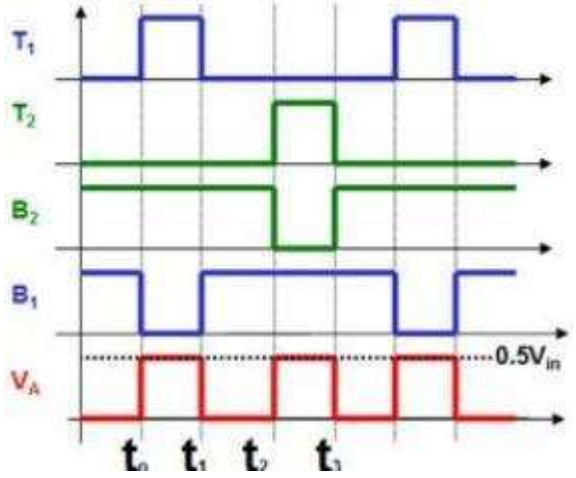

Fig 1.0 Basic Three level Buck Converter

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Flying capacitor three level buck converter topology

Three level buck converter works as a multilevel converter. The three level buck converters can offer high efficiency and high power density in voltage regulation and point of load applications. The gains are made possible by adding a flying capacitor that reduces the MOSFET voltage stress by half allowing for the use of low voltage devices, doubles the effective switching frequency, and decreases the inductor size by reducing the volt-second across the inductor. The flying capacitor three-level buck converter topology is illustrated in Fig.2.0

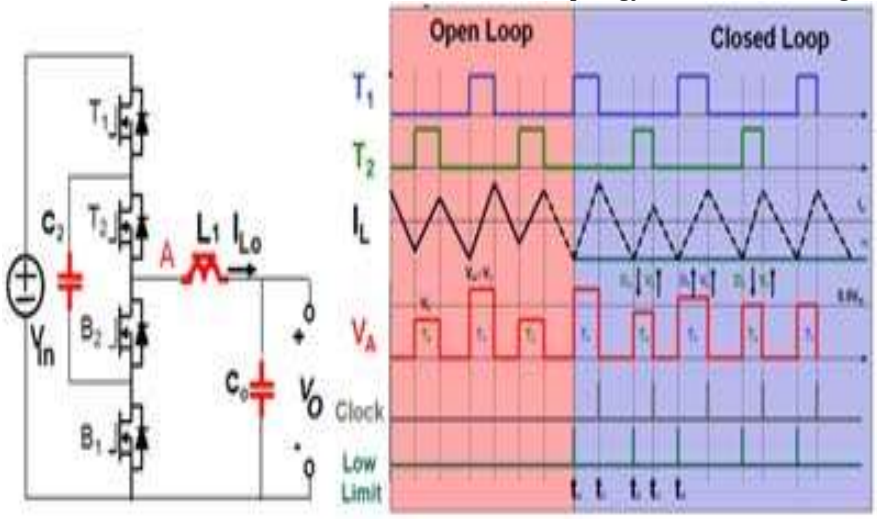

Fig 2.0 Flying Capacitor

Implementation of 3-level converter

Fig. 3 presents an overall block diagram comprising a set of thin-oxide transistors used as power FETs for power conversion, drive circuitry for the power FETs, a flying capacitor, an on-die LC filter, and control circuitry for voltage regulation. A relatively slow digital feedback loop sets the signals out of the digital pulse-width modulator (DPWM) that feed drivers to switch the 3-level converter with appropriate duty cycles ( ). In parallel, a fast shunt regulator [4] on the output reacts to sudden load current transients to maintain a steady voltage. The overall design target is to minimize conversion loss, on-die area overhead, voltage fluctuations, and dynamic voltage scaling time. This section further studies the components in Fig. 3 and looks at circuit implementations in detail. The 3-level converter uses four power FETs, a flying capacitor, and an output LC filter to generate a wide range of

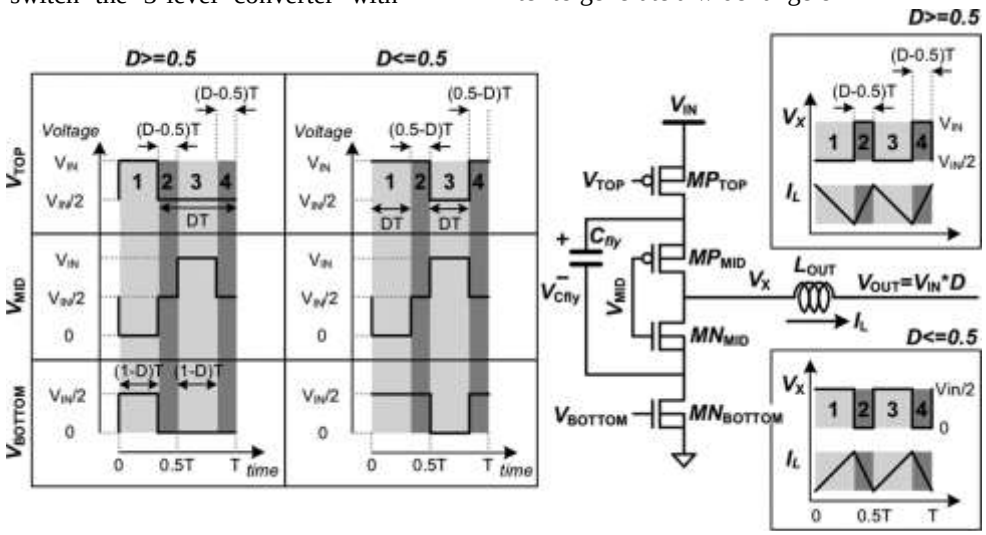

Fig 3.0 Schematic of the proposed 3-level power converter.

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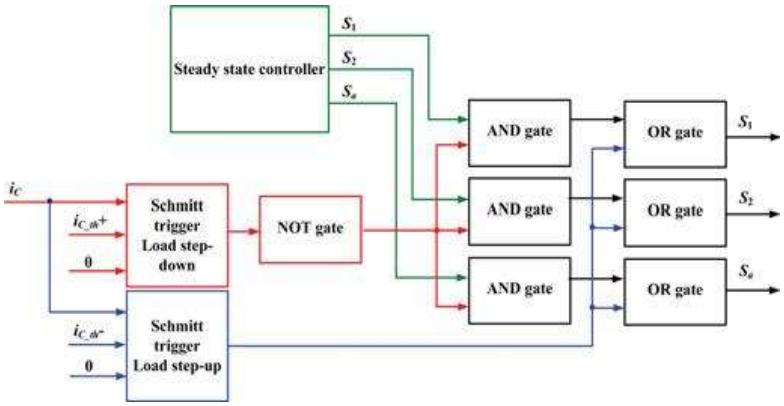
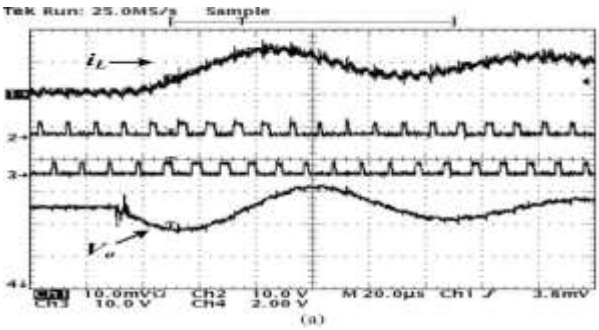
A Controller Design

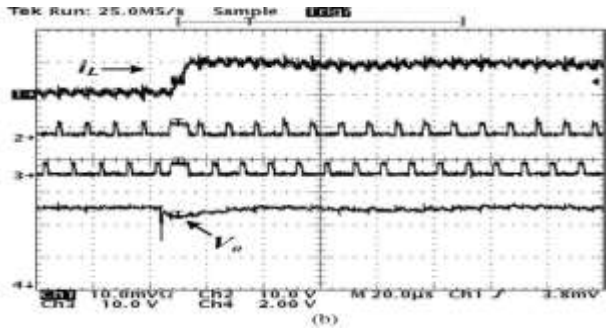


Simulation result

In order to verify the improvement in dynamic response of the modified flying capacitor buck converter with the proposed transient controller, a simulation model has been developed using PLECS of matlab/simulink. Both the simulation and experimental analysis are done for a low-power flying capacitor three-level buck converter as this topology has been proved to be attractive for low-power POL applications. Also, the proposed modified converter will be more useful in low power POL applications.

Key waveforms with transient control





Conclusion

A transient control strategy to improve the dynamic response of a flying capacitor three-level buck converter has been investigated in this paper. First, a flying capacitor three-level buck converter has been modified. Second, a transient controller for the modified flying capacitor three-level converter has been pro-posed. Simulation and hardware results show that the proposed approach can greatly improve the dynamic response for both load step-up and load step-down scenarios. Comparing with reported methods, the proposed controller takes advantages of both faster dynamic response performance and simpler control structure. Since the voltage deviations are much reduced by the proposed control strategy, the output filtering capacitor can be less that increases the system stability and reduces the system cost. As long as the efficiency is concerned, since the addi-tional power loss is only associated with the conduction losses, which is much smaller compared with the switching losses in high-frequency applications. The proposed method can be easily extended to other dc–dc converter topologies.

References

1. M. Cast illa, J. M. Guerrero, J. Matas, J. Miret, and J. Sosa, " Comparat ive st udy of hyst eret ic controllers for single-phase voltage regulat ors," IET Power Elect ron., vol. 1, no. 1, pp. 132– 143, Mar. 2008.
2. J. Zhao, T. Sato, T . Nabeshima, and T . Nakano, " St eady-state and dynamic analysis of a buck converter using a hysteret ic PWM control," in Proc. IEEE 35th Annu. Appl. Power Electron. Spec. Conf., Jun. 2004, vol. 5,pp. 3654–3658

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Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

3. K. K. S. Leung and H. S. Chung, "Dynamic hysteresis band control of the buck convert er with fast transient response," IEEE Trans. Circuits Syst . II, Exp. Briefs, vol. 52, no. 7, pp. 398–402, Jul. 2005.
4. A. Barrado, R. Vazquez, A. Lazaro, E. Olias, and J. P leit e, "Linear nonlinear cont rol applied to buck converters to get fast transient response," in Proc. IEEE Annu. Appl. Power Electron. Spec. Conf., 2004, pp. 999– 1003.
5. A. Barrado, R. Vazquez, A. Lazaro, J. Pleite, J. Vazquez, and E. Olias, "Newdc-dc converter with lowoutput voltage and fastt ransient response," in Proc. IEEE 18th Annu. Appl. Power Electron. Conf. Expo., Feb. 2003,pp. 432–437.
6. G. Feng, E. Meyer, and Y. F. Liu, " A new digit al cont rol algorithm to achieve opt imal dynamic performance in dc-to-dc converters," IEEE Trans. Power Elect ron., vol. 22, no. 4, pp. 1489–1498, Jul. 2007.
7. D. D. Lu, J. C. P . Liu, F. N. K. P oon, and B. M. H. Pong, "A single phase voltage regulator module with stepping inductance for fast t ransient response," IEEE Trans. Power Elect ron., vol. 22, no. 2, pp. 417–424, Mar.2007.